(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 October 2003 (16.10.2003)

PCT

(10) International Publication Number
WO 03/085730 A1

(51) International Patent Classification[7]: H01L 23/31

(21) International Application Number: PCT/IB03/01420

(22) International Filing Date: 8 April 2003 (08.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02076425.4 11 April 2002 (11.04.2002) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WEEKAMP, Johannus, W.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **VAN VEEN, Nicolaas, J.**, A. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

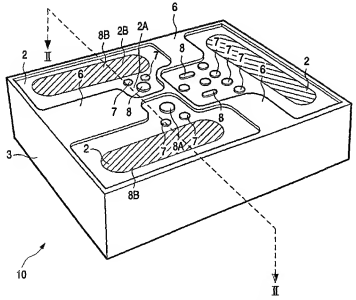
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) **Title:** METHOD OF MANUFACTURING AN ELECTRONIC DEVICE, AND ELECTRONIC DEVICE



(57) Abstract: The invention relates to a method of manufacturing a semiconductor device (10), whereby a electric element (11) is attached on or above a carrier plate (4) which comprises a first layer (5) of a first material and a second layer (2) of a second material which differs from the first, which is electrically conducting, which has a smaller thickness than the first layer (5), and in which a cavity (6) is formed that extends at least to the first layer (5). The element (11) is electrically connected to parts (2) of the carrier plate (4) at first connection regions (1), and an encapsulation is deposited around the element (11) and in the cavity (6). Then so much of the first layer (5) of the carrier plate (4) is removed that the cavity (6) is reached, whereby second connection conductors (2) are formed from the remaining portion of the carrier plate (4). According to the invention, at least one further cavity (7) is formed in a portion of the carrier plate (4) surrounded by the cavity (6) before the encapsulation (3) is deposited, which further cavity (7) becomes at least substantially filled with a portion of the encapsulation (3) during the deposition thereof and, within the second connection regions (2), separates a portion (2A) thereof from the remaining portion (2B) thereof, the smallest dimension of the portion (2A) being chosen to be smaller than the smallest dimension of the remaining portion (2B) of each second connection region (2). The portion (2A) may thus be readily provided with solder (8A) having a smaller thickness than the solder (8B) in the remaining portion of the second connection region (2). This is an advantage, for example in the case of surface mounting of the device (10). Preferably, the first connection regions (1) are connected to the portion (2A) of the connection region (2).

WO 03/085730 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Method of manufacturing an electronic device, and electronic device

The invention relates to a method of manufacturing an electronic device which comprises an electric element provided with first connection regions and with an electrically insulating envelope, which method comprises the steps of providing a recess in a first surface of a carrier plate, said plate comprising in that order a first layer of a first material and a second layer of a second, electrically conducting material different from the first material, which recess extends from the first surface through the second layer at least to the first layer; providing the electric element on or above the surface of the carrier plate; electrically connecting the first connection regions to portions of the second layer lying within the recess; surrounding the electric element by means of the insulating envelope which fills the recess in the carrier plate at least substantially; and removing the carrier plate from a second surface of the carrier plate, which second surface faces away from the first surface, to at least an extent such that the recess filled by a portion of the envelope is reached, whereby second connection regions are formed by the portions of the second layer lying within the recess.

The invention also relates to a semiconductor device comprising an electric element provided with first connection regions, further comprising second connection regions with a first side and with a second side facing away therefrom, which second connection regions are provided at the first side with an electrical connection to the first connection regions and can be provided at the second side with electrical connection pieces for placement on a substrate, which electric element is surrounded by an electrically insulating envelope which extends at least to the second connection regions.

Such a method is particularly suitable for the inexpensive manufacture of semiconductor devices among other items. The electric element therein is an electric element, such as a (semi-)discrete transistor or diode, an integrated circuit, a memory circuit, etc. The devices manufactured by such a method may also be particularly compact, which renders possible the ever advancing miniaturization required in many applications.

Such a method and such a semiconductor device are known from European patent EP 1 160 858 A2. It is described therein how a semiconductor IC (= Integrated Circuit) can be enveloped in a compact manner. The IC is fastened on or above a carrier plate. The first connection regions of the IC are connected to parts of the carrier plate either

directly or via an electrically conducting wire. The carrier plate comprises two metal layers in succession, of which the upper layer adjoining the IC has a smaller thickness than the lower layer. The carrier plate is provided with a recess which extends from the surface of the second layer into the first layer and which surrounds portions of the carrier plate from which the second connection regions of the enveloped IC will be formed. After the IC has been provided on or above the carrier plate, an electrically insulating (and passivating) envelope is provided around the IC and against the carrier plate. The recess is largely filled up with part of the envelope thereby. Then as large as possible a portion of the carrier plate is removed, in particular a major portion of the first layer thereof, such that the recess filled with a portion of the envelope is reached. The second connection regions of the enveloped IC are formed thereby from (remaining) portions of the carrier plate. The IC is then ready, for example, for final surface mounting or for fastening to a lead frame.

A disadvantage of the known method is that the solder provided as solder bumps on the second connection regions for final mounting will flow out over the entire connection region with a comparatively small and substantially homogeneous thickness after the necessary heating, and will thus remain present also after solidification. This may be avoided through the provision of a solder-repelling layer on the second connection regions, which layer is provided with openings by means of photolithography, in which openings the solder bumps are provided. This, however, makes the method more complicated. This is because said photolithography step has to take place during the assembling process, i.e. after the enveloping step. Such assembling processes, however, are often carried out in factories in which lithographic equipment is not present. In addition, a lithographic step requires an accuracy and time duration which are not available during assembling. An alternative reduction in size of the second connection regions does not provide a solution either, because this will cause the electrical and thermal quality of the connection of the IC to the outer world to deteriorate. This is also not desirable.

It is accordingly a first object of the invention to provide a method which does not have the above disadvantage, or at least to a lesser degree, and which is yet simple and accordingly inexpensive.

According to the invention, a method of the kind mentioned in the opening paragraph is for this purpose characterized in that the recess extends into the first layer, such that underetching takes place in the first layer with respect to the second layer under formation of a cavity, which cavity is filled up by the insulating envelope.

Etching down into the first layer creates a cavity below the second layer. This cavity is filled up by the insulating envelope. The edges of the second connection regions are provided thereby with a protective layer consisting of the insulating envelope. When the carrier plate is removed from the second surface, this protective layer will come to the surface. The second connection regions lie recessed with respect to said surface.

The method according to the invention has among its advantages that no lithographic step is necessary any more after enveloping; the second connection regions are in fact patterned into contact surfaces by means of the envelope. The properties of the electrically insulating envelope, which often comprises a synthetic resin such as an epoxy resin or a thermoplastic material, are such that solder is repelled thereby. The solder that is subsequently applied to the second connection regions thus remains restricted to the contact surfaces.

It is a further advantage of the method according to the invention that the second layer may be kept thin, in particular in comparison with the first layer. This has the result that second connection regions can be positioned at a smaller mutual distance than was possible in the prior art.

Finally, a major advantage of a method according to the invention is that it is comparatively simple and does not require an additional step.

In a favorable embodiment of the method, before the envelope is provided, at least one further recess is provided in a portion of the carrier plate surrounded by the recess, which further recess is substantially filled with a portion of the envelope during the provision thereof. Said further recess is positioned within the respective second connection region such that a portion thereof is delimited from the remaining portion of the second connection region, the smallest dimension of said portion being chosen to be smaller than the smallest dimension of the remaining portion of the second connection region. When the carrier plate is removed, so much of the carrier plate is removed that also the further recess is reached. Each second connection region formed is thus locally interrupted by a portion of the envelope present there. The properties of the electrically insulating envelope, which often comprises a synthetic resin such as an epoxy resin or a thermoplastic material, are such that solder is repelled thereby. It is true that the solder bump when provided at one side of the interruption of the second connection region will flow out during melting over the entire remaining portion of the second connection region, but after solidification it will remain present with a greater thickness in that portion of the connection region whose smallest dimension is greatest. Such a local elevation of the solder is particularly favorable, for example, for final

surface mounting of the semiconductor device. In addition, the electrical and thermal properties of the connection of the electric element to the outer world remain excellent because the surface of the total second connection region is hardly made smaller by the local interruption thereof, while also the electrical and thermal quality of the interconnection between the (two) parts of the second connection region thus formed remains excellent. This is very important, in particular in the case of comparatively compact semiconductor devices, even if the absolute power dissipation thereof is not great, because the power density increases in such devices.

In a preferred embodiment of a method according to the invention, therefore, a solder particle is provided on at least a portion of each second connection region after so much of the carrier plate has been removed that the recess and further recess have been reached and the second connection regions have been formed. Preferably, the solder particle is melted after its application such that each second connection region is wetted in its entirety, and such that the height of the solder in said portion of each second connection region is smaller than it is in the remaining portion of each second connection region after solidification of the solder owing to cooling-down.

In a major embodiment, the first connection regions are connected to said portions of the second connection regions. As a result, the connection between the first and the second connection region is not broken again or mechanically loaded during final mounting of the finished device by means of the thicker solder of the remaining portion of each second connection region. Preferably, furthermore, the recess and the further recess are simultaneously formed in one and the same process step. The method according to the invention is not more complicated or more expensive than the known method in that case. The use of an adapted mask suffices for achieving the desired result.

Preferably, the further recess is formed as one or several recesses in the carrier plate which are positioned within the respective second connection region to be formed such that they, together with a portion of the inner edge of the recess, delimit a portion of each second connection region whose smallest dimension is smaller than the smallest dimension of the remaining portion thereof. The ratio of the smallest dimension of the portion to that of the remaining portion of the second connection region is preferably chosen to be smaller than ½, and more preferably between 1/3 and 1/6. Very favorable results were obtained when aluminum was chosen for the material of the first layer of the carrier plate and copper for the material of the second layer of the carrier plate. These materials, and in particular copper, have good electrical and thermal properties and in addition can be very well, even selectively

etched with respect to one another, for example in a wet-chemical etchant. The removal of the major portion of the carrier plate may also very well be effected by means of CMP (= Chemical Mechanical Polishing).

Good results were obtained when the thickness of the first layer of the carrier plate was chosen to lie between 10 and 300 μm, and preferably at approximately 30 μm, and the thickness of the second layer was chosen to lie between 2 and 20 μm, preferably at 10 μm. It is advantageous to remove the first layer of the carrier plate in its entirety after the envelope has been provided. A very good etchant for aluminum - besides a possible use of CMP - is formed by hot sodium lye. The method according to the invention is particularly suitable for the manufacture of semiconductor devices with discrete or semi-discrete electric elements such as used, for example, in mobile telephones. The invention also relates to semiconductor devices obtained by a method according to the invention.

It is a second object of the invention to provide a semiconductor device of the kind mentioned in the second paragraph which can be manufactured in an inexpensive manner and in which the second connection regions are effective protected.

This second object is achieved in that the envelope extends to the second side of the second connection regions such that the second connection regions are accessible in a recess of the envelope for being placed on the substrate. The second connection regions in the semiconductor device according to the invention lie in a recess of the envelope, i.e. recessed with respect to the surface of the semiconductor device. The semiconductor device thus complies with the requirements for placement on a substrate, while no additional layers are necessary for this.

The electrical connection in the semiconductor device is preferably formed by bumps, but it may alternatively be realized with solder, bonding wires, or anisotropically conducting glue. It is furthermore possible to realize the connection in a contactless manner, for example by capacitive coupling, in particular for electric elements in which the number of incoming and outgoing signals and the power dissipation are comparatively limited, such as those used for identification purposes.

The connection pieces for placement on a substrate are preferably solder bumps. Alternatively, anisotropically conducting glues or other connection pieces may be used.

In a favorable embodiment, the device is provided with second connection regions of varying size on which the solder bumps, when applied as electrical connection pieces, will have a height which is dependent on the size of the respective second connection

region. The use of solder bumps of varying heights is found to be a very desirable characteristic of an envelope in practice. This may be realized in a simple manner in the device according to the invention thanks to the repelling action of the envelope with respect to solder.

The invention will now be explained in more detail with reference to an embodiment and the drawing, in which

Fig. 1 diagrammatically and in perspective view shows a semiconductor device manufactured by a method according to the invention,

Fig. 2 shows the device of Fig. 1 in a diagrammatic cross-sectional view taken on the line II-II in the thickness direction, and

Figs. 3 to 9 show the device of Fig. 1 in consecutive stages of manufacture by an embodiment of a method according to the invention in a diagrammatic cross-sectional view taken on the line II-II in the thickness direction.

The Figures are not true to scale, and some dimensions have been particularly exaggerated for greater clarity. Corresponding regions or components have been given the same reference numerals as much as possible.

Fig. 1 is a diagrammatic perspective view of a semiconductor device manufactured by a method according to the invention. Fig. 2 also shows the device of Fig. 1, in a diagrammatic cross-sectional view taken on the line II-II in the thickness direction. Figs. 2 to 5 are diagrammatic cross-sectional views taken on the line II-II in the thickness direction in Fig. 1 of the device of Fig. 1 in consecutive stages of its manufacture by means of an embodiment of a method according to the invention. The device 10 comprises an electric element 11 (see Fig. 2) which is provided with a plurality, three in this case, of first connection regions 1, two of which are depicted in Fig. 2, and which is surrounded by an envelope 3, made of epoxy material in this case. A second connection region 2 for each first connection region 1 is present on the envelope 3 and is connected thereto by means of solder 12. The electric element 11 in this example comprises a bipolar transistor 11 and is accordingly provided with three second connection regions 2, as can be seen at the upper side. Said regions are provided with solder 8.

The second connection regions 2 are surrounded by portions 6 of the envelope 3, and portions 7 of the envelope 3 lie within the second connection regions 2. The solder 8 extends over each entire second connection region 2, but it has a greater thickness locally (see Fig. 2). Since portions 2A of the second connection regions 2 are delimited from the remaining portion 2B of the second connection regions 2 by portions 7 of the envelope 3 and by a portion of the inner edge of the portions 6 of the envelope 3, a solder bump 8 placed in the second connection region 2 has indeed wetted the entire second connection region 2 after melting but, after solidification of the solder 8, the thickness of the portion 8A of the solder 8 lying on the portion 2A will be smaller than the thickness of the portion 8B of the solder 8 lying on the remaining portion 2B. This is also because the smallest dimension of the portion 2A is smaller than the smallest dimension of the remaining portion of the second connection region. This difference in thickness of the solder 8 is favorable for surface mounting of the device 10.

Figs. 3 to 9 are diagrammatic cross-sectional views taken on the line II-II in the thickness direction in Fig. 1 showing the device of Fig. 1 in consecutive stages of manufacture by an embodiment of a method according to the invention.

The method starts, see Fig. 3, with a carrier plate 4 which comprises a first layer, of aluminum in this case and 30 μm thick. A second layer 2 of an electrically conducting material, copper in this case, and with a thickness smaller than that of the first layer 5, 10 μm in this case, is present thereon. In this assembly, see Fig. 4, the beginning of a recess 6 and of a further recess 7, i.e. two further, round recesses 7, are formed by means of photolithography and etching. The etchant used may be, for example, ferrichloride which etches copper more or less selectively with respect to aluminum. Subsequently, see Fig. 5, the formation of the recess 6 and of the further recess 7 is continued in that the first layer 5 of the carrier plate 4 is etched. Aluminum may be selectively etched with respect to copper, for example, by means of sodium lye. In this manner the aluminum of the first layer 5 is underetched with respect to the portions 2A, 2B of the copper layer 2.

Subsequently, see Fig. 6, an electric element 11, a bipolar transistor 11 in this case, is fastened on or above, in this case on the carrier plate 4. This is done here by means of solder 12, with which the electric element 11 is fastened by its connection regions 11 to the portions 2A, 2B of the carrier plate 4. The electric element 11 may be fastened to the carrier plate 4 in an alternative manner, for example by means of an electrically insulating glue. The connection regions 1 of the element 11 are then preferably turned so as to face away from the

carrier plate 4 and are electrically connected to the portions 2A, 2B of the carrier plate 4 by means of conductive wires.

After this, see Fig. 7, the device 10 is placed in a mold (not shown) and an envelope 3 comprising an epoxy resin material in this case, is provided around the element 11 and pressed against the carrier plate 4 by means of injection molding. The recess 6 and the further recess 7 are thus filled with portions 6, 7 of the envelope 3. Subsequently, see Fig. 8, a major portion of the carrier plate 4 is removed, by means of CMP (= Chemical Mechanical Polishing) in this case. This continues until the recess 6 and further recess 7 filled with portions of the envelope 3 have been reached. In the present example, the final remnants of the first layer 5 still present between the portions 6 and 7 of the envelope 3 are then removed in an etching process, for example by means of the selective etchant for aluminum mentioned above.

Thus, according to the invention, a smaller portion 2A - at least as regards the smallest dimension - is delimited within each second connection region 2 from the larger remaining portion 2B of each second connection region. The delimitation of the portion 2A is formed on the one hand by the inner edge of the portion 6 of the envelope 3 surrounding the second connection region 2, and on the other hand by the portions 7, two portions here, of the envelope 3 formed within the second connection region 2.

After the solder bump 8, see Fig. 9, has been placed on the portion 2B of the second connection region 2, for example, and has been melted, the solder 8 will flow out over the entire second connection region 2 before it solidifies again owing to cooling down, but the thickness of the solder 8A in the portion 2A of the second connection region 2 will be smaller than in the portion 2B thereof. The electrical and thermal qualities of the portions 2A, 2B are substantially the same here as in the case in which the portions 7 of the envelope 3 are not present within each second connection region 2. This is true in particular thanks to the fact that the portions 6 and 7 of the envelope 3 extend partly above the second connection region 2, so that the surface area thereof is not or at least substantially not reduced. The result is a particularly compact semiconductor device 10 which is highly suitable for surface mounting and which also has very favorable thermal and electrical properties. It is of particular advantage here that the first connection regions 1 of the element 1 in this example are connected to the portion 2A of the second connection region 2, where the solder thickness is smallest. It is noted that Fig. 9 shows the same assembly as Fig. 2, but Fig. 9 has been rotated through 180° in the plane of drawing with respect to Fig. 2. This is connected with the

manufacture of the device 10 described with reference to Figs. 3 to 9, which makes such a representation logical.

The following should be noted with respect to the dimensions of the device 10 whose manufacture was described above. The dimensions of the electric element 11 are 350 x 350 μm^2. Its thickness is approximately 200 μm. The entire device 10 measures 1000 x 800 x 230 μm^3. The fact that the entire device 10 is larger than the element 11 has the advantage that the device can be positioned more easily by means of a placement machine, for example during final mounting. The thickness of the solder 8A is, for example, 30 μm, and that of the solder 8B 150 μm. The smallest dimensions of the portion 2A and of the remaining portion 2B of each second connection region 2 are approximately 30 and 180 μm, respectively. These are the dimensions measured along the line II-II in Fig. 1 in the present example. The portion 2A, furthermore, is approximately square, and the greatest dimension of the remaining portion 2B of each second connection region is approximately 600 μm.

The invention is not limited to a method as described for the embodiment, since many variations and modifications are possible to those skilled in the art within the scope of the invention. Thus devices may be manufactured with different geometries and/or different dimensions. It is also possible to use alternative materials, especially for the carrier plate.

It is further noted that a large number of devices can be manufactured simultaneously by the method according to the invention, although the manufacture of a single device only is described and depicted for the embodiment. Individual semiconductor devices may then be obtained by mechanical separation techniques such as sawing, cutting, or breaking. In an attractive modification, another recess is formed between two adjoining devices in the carrier plate. When the envelope is provided over the element in the form of a drop of liquid, this liquid will wet the carrier plate and the element up to the edge of the other recess. The liquid may then be cured. When the carrier plate is removed, the individual devices will then automatically become separated.

Besides semiconductor devices with a discrete element, as in the example, smaller, semi-discrete ICs, for example comprising 1 to 100 active and/or passive elements, may alternatively be manufactured. An application to larger, more complicated ICs is also advantageously possible. Another advantageous possibility is to use a filter or one or several passive elements as the electric element.

It is finally noted that the second connection region may be given a geometry other than that shown in the examples. Thus both the portion and the remaining portion of

said region may have approximately a circular geometry, the circles being interconnected by one or several narrower portions. It will be obvious that in this case the smallest dimension both of the portion and of the remaining portion of the second connection region will be equal to the diameter of the respective portion and remaining portion of the second connection region. The further recesses need not be round, as in the example, but may have some other geometry.

CLAIMS:

1. A method of manufacturing an electronic device (10) which comprises an electric element (11) provided with first connection regions (1) and with an electrically insulating envelope (3), which method comprises the steps of:

- providing a recess (6) in a first surface of a carrier plate (4), said plate (4) comprising in that order a first layer (5) of a first material and a second layer (2) of a second, electrically conducting material different from the first material, which recess (6) extends from the first surface through the second layer (2) at least to the first layer (5);
- providing the electric element (11) on or above the surface of the carrier plate (4);
- electrically connecting the first connection regions (1) to portions (2A, 2B) of the second layer (2) lying within the recess (6);
- surrounding the electric element (11) by means of the insulating envelope (3) which fills up the recess (6) in the carrier plate (4) at least substantially; and
- removing the carrier plate (4) from a second surface of the carrier plate (4), which second surface faces away from the first surface, to at least an extent such that the recess (6) filled by a portion of the envelope (3) is reached, whereby second connection regions (2) are formed by the portions (2A, 2B) of the second layer (2) lying within the recess (6),
- characterized in that the recess (6) extends into the first layer (5), such that underetching takes place in the first layer (5) with respect to the second layer (2) under formation of a cavity, which cavity is filled up by the insulating envelope (3).

2. A method as claimed in claim 1, characterized in that, before the envelope (3) is provided, at least one further recess (7) is provided in a portion of the carrier plate (4) surrounded by the recess (6), which further recess (7) is largely filled with a portion of the envelope (3) during the application thereof, and which further recess (7) is positioned within each second connection region (2) such that a portion (2A) thereof is delimited from the remaining portion (2B) of the second connection region (2), the smallest dimension of said portion (2A) being chosen to be smaller than the smallest dimension of the remaining portion

(2B) of the second connection region (2), and so much of the carrier plate (4) is removed that also said further recess (7) is reached.

3. A method as claimed in claim 1, characterized in that a solder particle (8) is provided on at least a portion of each second connection region (2) after so much of the carrier plate (4) has been removed that the recess (6) and the further recess (7) have been reached and the second connection regions (2) have been formed.

4. A method as claimed in claim 3, characterized in that the solder particle (8) is melted after its application such that each second connection region (2) is wetted in its entirety, and such that the height of the solder (8A) in said portion (2A) of each second connection region (2) is smaller than it is of the solder (8B) in the remaining portion (2B) of each second connection region (2) after solidification of the solder (8) owing to its cooling down.

5. A method as claimed in claim 2, characterized in that the first connection regions (1) are connected to said portions (2A) of the second connection regions (2).

6. A method as claimed in claim 2, characterized in that the recess (6) and the further recess (7) are formed in one and the same process step.

7. A method as claimed in claim 2, characterized in that the further recess (7) is made in the form of one or several recesses (7) in the carrier plate (4) which are positioned within each second connection region (2) under formation such that they together with part of the inner edge of the recess (6) surround a portion (2A) of each second connection region (2), of which portion (2A) the smallest dimension is smaller than the smallest dimension of the remaining portion (2B) of each second connection region (2).

8. A method as claimed in claim 2, 7, or 8, characterized in that the ratio of the smallest dimension of the portion (2A) to that of the remaining portion (2B) of the second connection region (2) is preferably chosen to be smaller than ½, more preferably between 1/3 and 1/6.

9. A method as claimed in any one of the preceding claims, characterized in that aluminum is chosen for the material of the first layer (5) of the carrier plate (4), and copper is chosen for the material of the second layer (2) of the carrier plate (4).

10. A semiconductor device (10) comprising an electric element (11) provided with first connection regions (1), further comprising second connection regions (2) with a first side and with a second side facing away therefrom, which second connection regions (2) are each provided at the first side with an electrical connection to the first connection regions (1) and can be provided at the second side with electrical connection pieces for placement on a substrate, which electric element (11) is surrounded by an electrically insulating envelope (3) which extends at least to the second connection region (2), characterized in that the envelope extends to the second side of each second connection region (2) such that the second connection region is accessible in a recess of the envelope (3) for being placed on the substrate.

11. A semiconductor device (10) as claimed in claim 10 and provided with second connection regions (2) of varying size, whereon, when solder bumps (8)are used as the electrical connection pieces, said bumps (8) will have a height which is dependent on the size of the respective second connection regions (2).

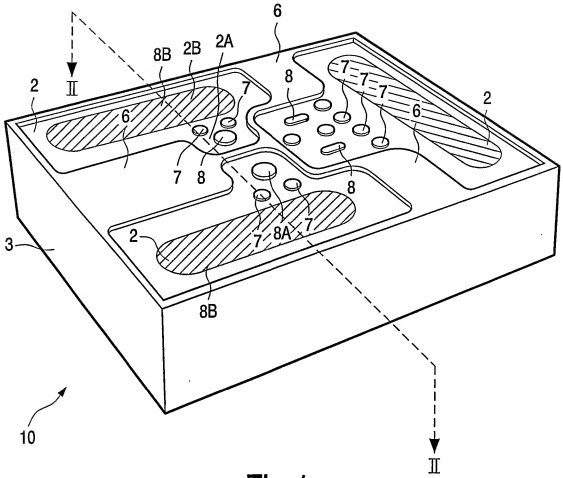

6
8B
2B
2A
2
II
8
7
7
7
7
6
6
2
7
8
8
2
7
8A
7
3
8B
10
II

Fig.1

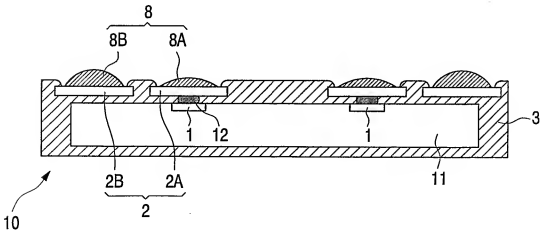

8
8B
8A
1
12
1
3
2B
2A
11
2
10

Fig.2

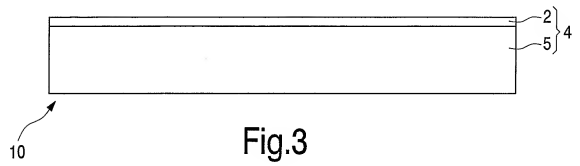


Fig.3

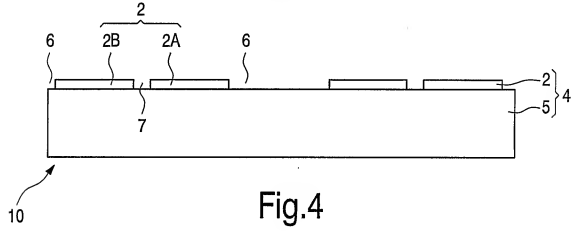


Fig.4

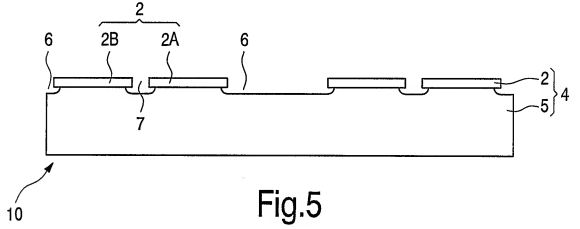


Fig.5

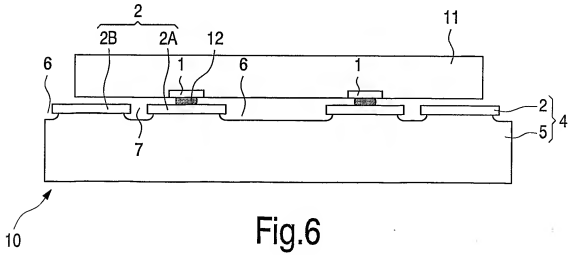


Fig.6

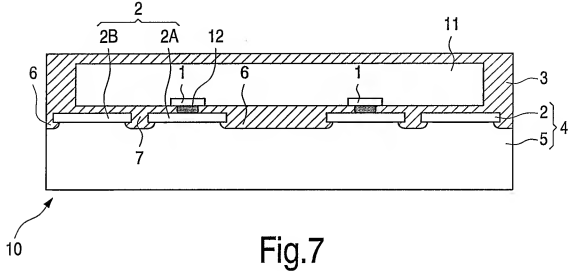


Fig.7

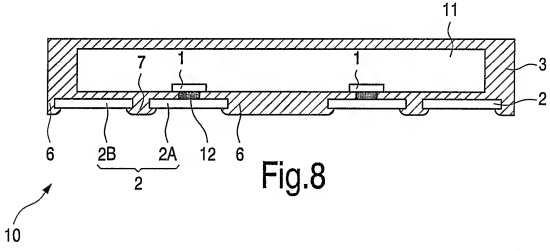


Fig.8

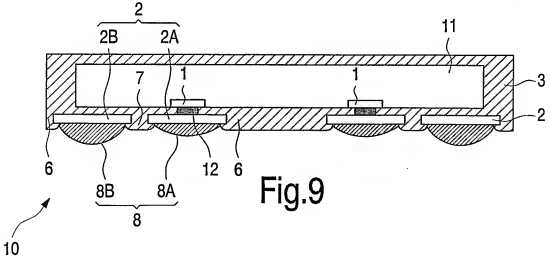


Fig.9

INTERNATIONAL SEARCH REPORT

Internatic _ plication No
PCT/IB 03/01420

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 187 205 A (SANYO ELECTRIC CO) 13 March 2002 (2002-03-13) page 5, column 7, line 23 - page 6, column 9, line 35; figures 2-6	1,3,10
X	EP 1 143 509 A (SANYO ELECTRIC CO) 10 October 2001 (2001-10-10) the whole document	1,2,6,7, 10
X	PATENT ABSTRACTS OF JAPAN vol. 0090, no. 69 (E-305), 29 March 1985 (1985-03-29) & JP 59 208756 A (SONY KK), 27 November 1984 (1984-11-27)	1
A	the whole document -& JP 59 208756 A (SONY KK) 27 November 1984 (1984-11-27)	10

-/-

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 2003	11/08/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zeisler, P.

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 11, 30 September 1999 (1999-09-30) & JP 11 163024 A (SUMITOMO METAL MINING CO LTD), 18 June 1999 (1999-06-18) abstract; figures 5,6 -& JP 11 163024 A (SUMITOMO METAL MINING CO LTD) 18 June 1999 (1999-06-18)	1,10

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1187205 A	13-03-2002	JP 2002083903 A	22-03-2002
		CN 1341963 A	27-03-2002
		EP 1187205 A2	13-03-2002
		US 2002048828 A1	25-04-2002
EP 1143509 A	10-10-2001	JP 2001250883 A	14-09-2001
		JP 2001250884 A	14-09-2001
		CN 1315823 A	03-10-2001
		EP 1143509 A2	10-10-2001
		US 6562660 B1	13-05-2003
JP 59208756 A	27-11-1984	JP 1760995 C	20-05-1993
		JP 4047977 B	05-08-1992
JP 11163024 A	18-06-1999	NONE	